
CGB (Color Game Boy)
User's Guide

Ver.1-3

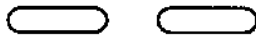
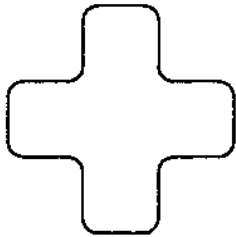


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CGB System

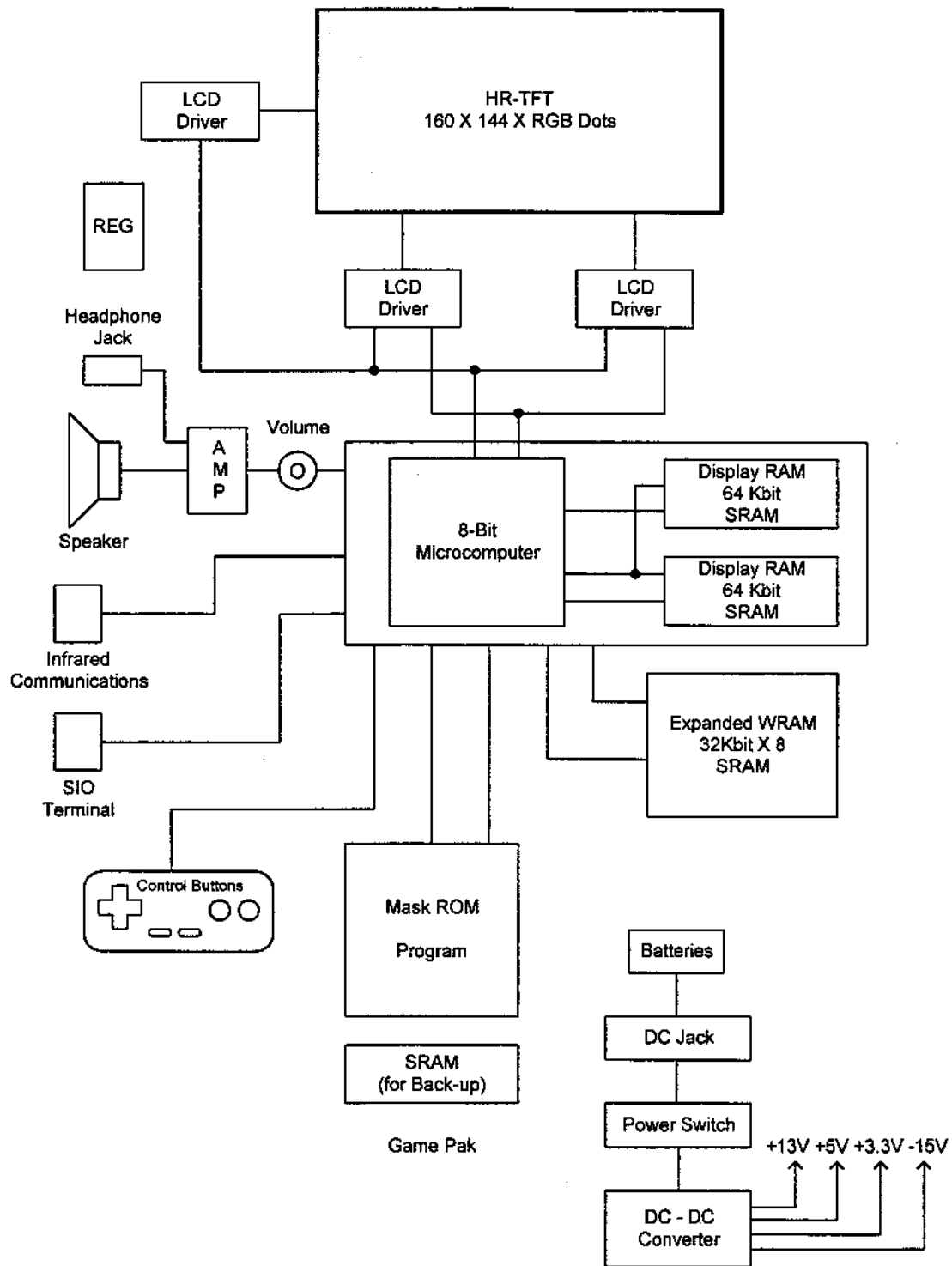
System Configuration

- The CGB (Color GameBoy) is a portable game machine which realizes color display while providing full compatibility with the existing GameBoy software. With a reflective color liquid crystal, display size and battery life nearly equivalent to those of the current MGB (Pocket GameBoy) can be maintained. Even higher speed processing than that of the current DMG becomes possible using the expanded functions.
- The CGB System is constructed around a CPU with a built-in LCD controller which was designed for the CGB (CGB-CPU).
- The System includes the following:
 - ◆ Color dot matrix LCD unit capable of displaying 32 gradient levels each of R, G, and B
 - ◆ DC-DC power converter
 - ◆ Sound amplifier
 - ◆ 128-Kbit SRAM (for LCD display)
 - ◆ 256-Kbit SRAM (for game unit work RAM)
 - ◆ Control Buttons
 - ◆ Speaker
 - ◆ Headphone Jack
 - ◆ DC Power Jack
 - ◆ Serial communications connector (6-pin sub-connector)
 - ◆ Infrared communication element (photo-Tr, photo-LED)
- A 32-pin connector is built-in for the Game Pak.
- The CGB System features the following operating modes.
 - ◆ DMG/MGB Mode (When using a DMG-dedicated Game Pak)
 - The new CGB register, expanded memory area, and new functions will not work.
 - Automatically selects color data consistent with the old BGP, OBP0, and OBP1 palettes.
 - ◆ CGB Mode (When using a CGB-compatible or CGB-dedicated Game Pak)
 - The new CGB register, expanded memory area, and new functions can be used.

NOTE: A special code must be set in the ROM registration area in order to switch to the CGB mode. (Refer to "Specifications of Data Registered in ROM" on page A-1.)

- The following Game Pak(s) will work with the CGB System.
 - ◆ DMG-dedicated Game Pak (conventional DMG/MGB Game Pak)
 - ◆ CGB-compatible Game Pak (DMG/MGB-compatible Game Pak that will work in CGB Mode)
 - ◆ CGB-dedicated Game Pak (special Game Pak made to work in CGB Mode)

System Configuration



Comparison of DMG/MGB

Functional Comparison

Item	DMG/MGB-CPU	CGB-CPU
CPU Operating Speed (System Operating Frequency)	1.05 Mhz	1.05 MHz 2.10 MHz Switchable
Game RAM Work & Stacks Game Unit Work OAM LCD Display	127 x 8 bits 8,192 bytes 40 x 28 bits 8,192 bytes	127 x 8 bits 32,768 bytes 40 x 32 bits 16,384 bytes
Game Pak Memory Space ROM RAM	32,768 bytes 8,192 bytes	32,768 bytes 8,192 bytes
LCD Controller Display Capacity Block Configuration BG, Window side OBJ side No. of Simultaneous Characters BG OBJ for 8 x 8 for 8 x 16 Gradations BG, Window side Gradations OBJ side OBJ Priority Order X coordinates are different X coordinates are the same	160 x 144 dots 8 x 8 dots 8 x 8 or 8 x 16 dots 256 types 256 types 128 types 4 gradations 1 palette 3 gradations 2 palettes OBJ with lower X coordinate OBJ with newest OBJ No.	160 x 144 x RGB dots 8 x 8 dots 8 x 8 or 8 x 16 dots 512 types 512 types 256 types 4 colors 8 palettes (DMG/MGB Mode - 4 colors 1 palette) 3 colors 8 palettes (DMG/MGB Mode - 3 colors 2 palettes) OBJ with newest OBJ No. (OBJ with lower X coordinate in DMG/MGB Mode) OBJ with newest OBJ No.
Timer & Divisions	8-bit timer x 1 16 level division x 1	8-bit timer x 1 16 level division x 1
Serial Input/Output Baud Rate	8 bits x 1 8 K	8 bits x 1 8K/256K (2X-speed mode - 16K/512K)
DMA Controller Old DMA Horizontal Blank DMA General Purpose DMA	No. 0000 ~ DFFF → OAM — ---	No. 0000 ~ DFFF → OAM Cartridge & Work RAM → VRAM Cartridge & Work RAM → VRAM
Interrupt Functions Internal Interrupt External Interrupt	4 types (maskable) 1 type (maskable)	4 types (maskable) 1 type (maskable)
Input/Output Ports		

Serial I/O Port Infrared Comm. Port	SIN, SCK, SOUT ---	SIN, SCK, SOUT Software controllable
Sound Output Circuit	4 types of sounds	4 types of sounds Monaural (VIN) external sound, mixable input

Register Comparison

Application	DMG/MGB-CPU		CGB-CPU	
	Register Name	Address	Register Name	Address
Port Mode Register	P1	FF00	P1	FF00
	SB	FF01	SB	FF01
	SC	FF02	SC	FF02
	DIV	FF04	DIV	FF04
	TIMA	FF05	TIMA	FF05
	TMA	FF06	TMA	FF06
	TAC	FF07	TAC	FF07
	—	—	KEY1	FF4D
	—	—	RP	FF56
—	—	SVBK	FF70	
Interrupt Flags	IF	FF0F	IF	FF0F
	IE	FFFF	IE	FFFF
	IME		IME	
LCD Display Register	LCDC	FF40	LCDC	FF40
	STAT	FF41	STAT	FF41
	SCY	FF42	SCY	FF42
	SCX	FF43	SCX	FF43
	LY	FF44	LY	FF44
	LYC	FF45	LYC	FF45
	DMA	FF46	DMA	FF46
	BGP	FF47	BGP	FF47
	OBP0	FF48	OBP0	FF48
	OBP1	FF49	OBP1	FF49
	WY	FF4A	WY	FF4A
	WX	FF4B	WX	FF4B
	—	—	VBK	FF4F
	—	—	HDMA1	FF51
	—	—	HDMA2	FF52
	—	—	HDMA3	FF53
	—	—	HDMA4	FF54
	—	—	HDMA5	FF55
	—	—	BCPS	FF68
	—	—	BCPD	FF69
	—	—	OCPS	FF6A
	—	—	OCPD	FF6B
	OAM	FE00 ~ FE9F	OAM	FE00 ~ FE9F
Sound Register	NR x x	FF10 ~ FF26	NR x x	FF10 ~ FF26
	Wave RAM	FF30 ~ FF3F	Wave RAM	FF30 ~ FF3F

CGB Memory

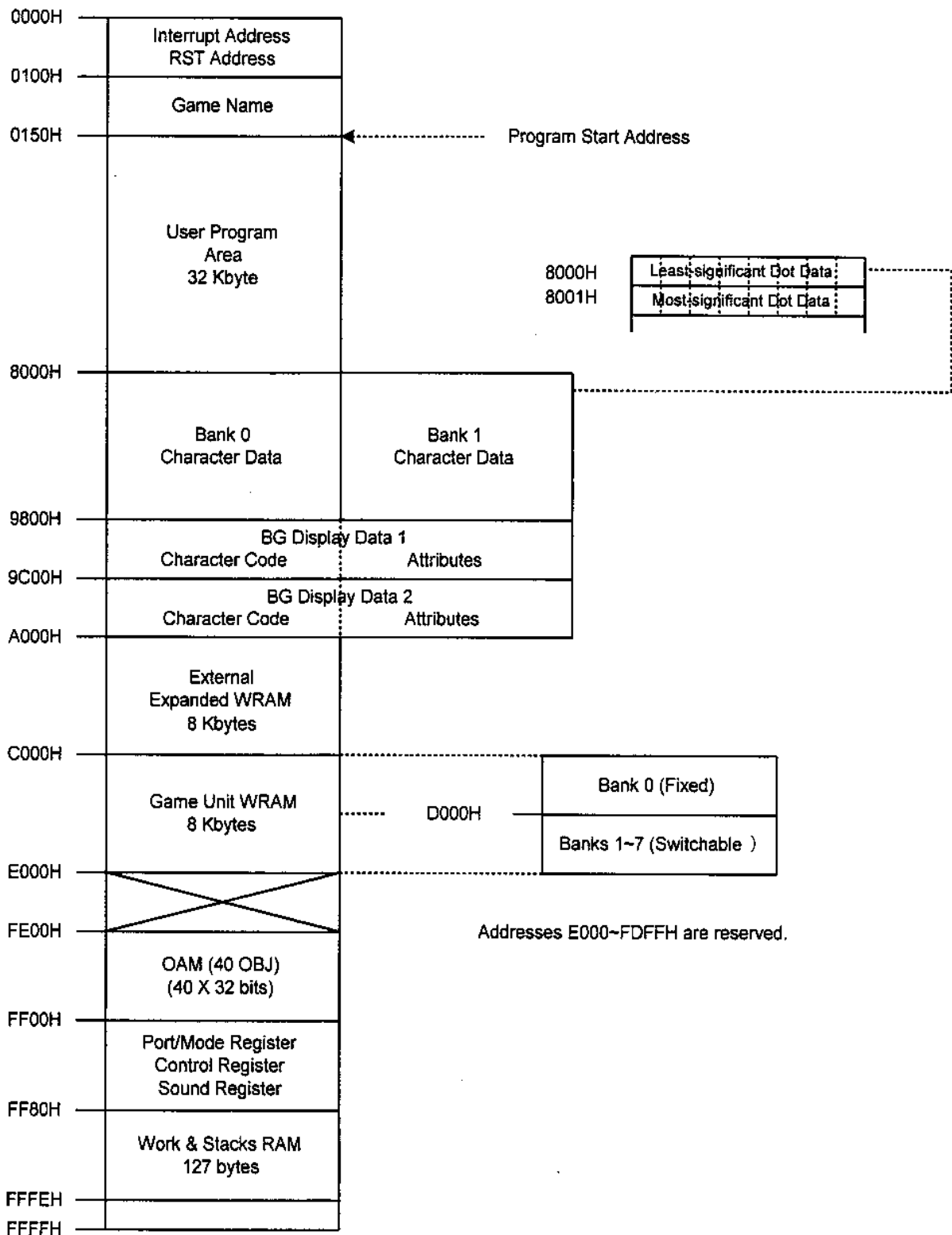
Memory Configuration

- 32 Kbytes, addresses 0~7FFFH, are provided in the CGB as the program area.
 - Addresses 000 ~ 0FFFH : Allocated for RST command jump destination addresses and interrupt start addresses.
 - Addresses 100 ~ 14FFH : Allocated as area for storing game name, etc.
 - Address 150H : Allocated as user's program start address.
- The 16 Kbytes (8 Kbytes x 2) are allocated for the LCD display RAM which is built into the system. A total of 8 Kbytes (addresses 8000~9FFFH) are used as the 8 Kbyte unit bank-switching memory for this RAM. The RAM area is also sub-divided into the following two areas.
 - 1) Character data storage area
 - 2) BG (background screen) display data (character codes, attributes) storage area
- 8 Kbytes, addresses A000~BFFFH, are allocated as the external expansion RAM area.
- A 32 Kbyte work RAM, addresses C000~DFFFH, is also built-in.

The RAM area is sub-divided into two areas in 4 Kbyte units. Up to 7 banks can be designated, not including the most-significant 4 Kbytes, and this can be used as a maximum 32 Kbyte memory space.

 - 1) 4 Kbytes (addresses C000~CFFFH) are fixed as bank 0.
 - 2) 4 Kbytes (addresses D000~DFFFH) can be designated as banks 1~7.
- Addresses E000~FDFFH are reserved.
- The internal RAM of the CGB-CPU is assigned to addresses FE00~FFFFH.
 - Addresses FE00~FE9FH : OAM-RAM (stores 40 OBJ's worth of display data)
 - Addresses FF00~FF7FH : Designated for command registers, flags, for
 - Address FFFFH : system control.
 - Addresses FF80~FFFEH : Used as CPU work RAM and stack RAM.

Memory Map



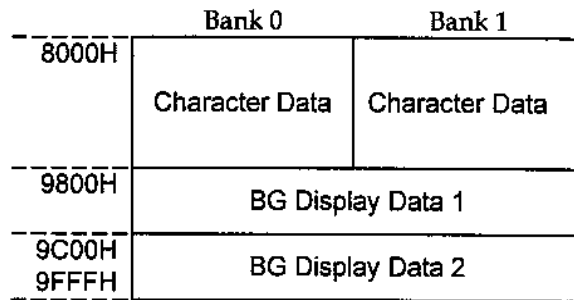
LCD Display RAM

An 8 kiloword (128 Kbit) LCD display RAM is built into the CGB-CPU.

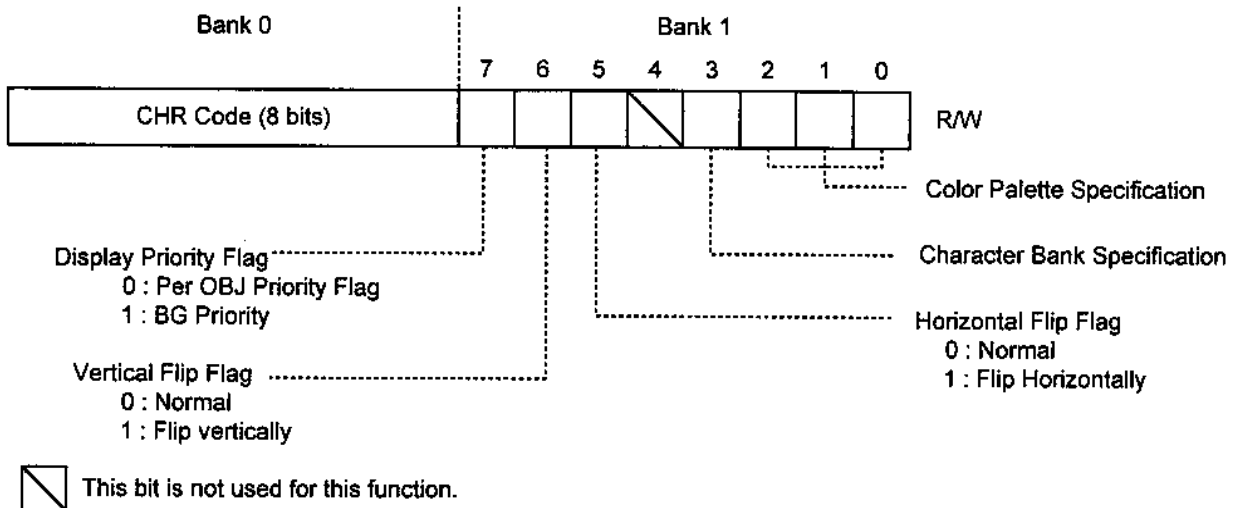
The LCD display RAM must perform bank-switching by means of the VBK register (address FF4FH) in order to connect the 16 Kbyte memory to the 8 Kbyte (64 Kbit) memory space in addresses 8000~9FFFH.

LCD Display RAM Mapping

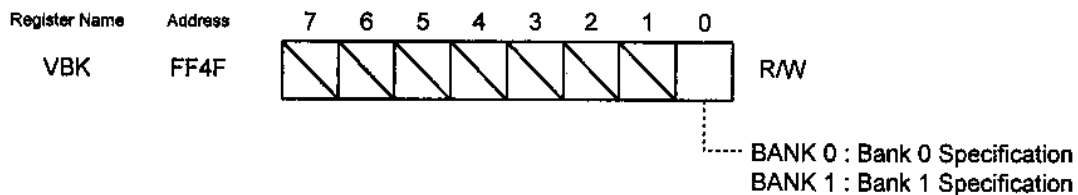
The 16 Kbyte memory space is divided by the VBK register into 2 x 8 Kbytes.



BG (Background Screen) Display Data



LCD Display RAM Bank Register



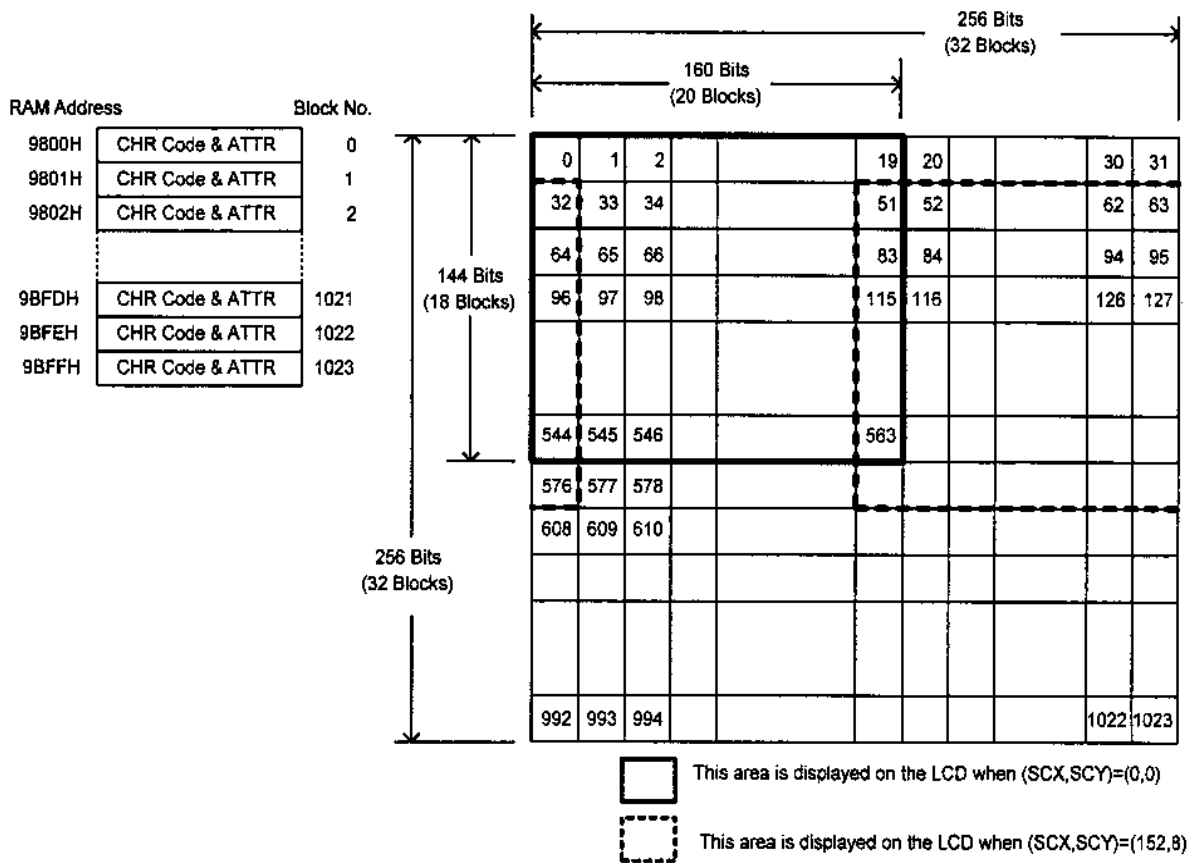
Bank 0 is selected immediately after the reset signal is canceled.

Correlation Between BG (Background Screen) Data and LCD Screen

It is possible to hold a total of 2 screens of BG display data as Data 1 and Data 2. Selecting whether to assign the BG display data to addresses 9800~9BFFH, or to assign them to addresses 9C00~9FFFH, is accomplished by bit 3 of the LCDC register.

	Bank 0	Bank 1
9800H	BG Display Data 1	
9C00H 9FFFH	BG Display Data 2	

1) When BG display data are assigned to addresses 9800~9BFFH



2) When BG display data are assigned to addresses 9C00~9FFFH

RAM Address	Block No.
9C00H	CHR Code & ATTB 0
9C01H	CHR Code & ATTB 1
9C02H	CHR Code & ATTB 2
9FFDH	CHR Code & ATTB 1021
9FFEH	CHR Code & ATTB 1022
9FFFH	CHR Code & ATTB 1023

Character Code Mapping

Twice the number of characters can be stored in the LCD display RAM of the CGB than in existing DMG/MGB. Presently, banks 0 and 1 are mapped in the same way as in DMG/MGB.

1) When BG character data are assigned to addresses 8800~97FFH

- When BG and OBJ are both 8 x 8 dots/block

CHR Code	Address	Bank 0	Bank 1
X00	8000H	OBJ Code "000"	OBJ Code "100"
	800FH	Dot Data	Dot Data
X01	8010H	OBJ Code "001"	OBJ Code "101"
	801FH	Dot Data	Dot Data

X80	8800H	OBJ Code & BG Code "080"	OBJ Code & BG Code "180"
	880FH	Dot Data	Dot Data
X81	8810H	OBJ Code & BG Code "081"	OBJ Code & BG Code "181"
	881FH	Dot Data	Dot Data

Area shared by OBJ and BG			
XFE	8FE0H	OBJ Code & BG Code "0FE"	OBJ Code & BG Code "1FE"
	8FEFH	Dot Data	Dot Data
XFF	8FF0H	OBJ Code & BG Code "0FF"	OBJ Code & BG Code "1FF"
	8FFFH	Dot Data	Dot Data

X00	9000H	BG Code "000"	BG Code "100"
	900FH	Dot Data	Dot Data

X7F	97F0H	BG Code "07F"	BG Code "17F"
	87FFH	Dot Data	Dot Data

CHR Codes:

OBJ 256 x 2 type

BG 256 x 2 type

■ For 8 x 16 dots/block (OBJ) and 8 x 8 dots/block (BG)

CHR Code	Address	Bank 0	Bank 1
X00	8000H		
X01	800FH	OBJ Code "000"	OBJ Code "100"
	8010H	Dot Data	Dot Data
X02	801FH		
	8020H		
X03	802FH	OBJ Code "002"	OBJ Code "102"
	8030H	Dot Data	Dot Data
	803FH		
X80	8800H	OBJ Code "080" & BG Code "080"	OBJ Code "180" & BG Code "180"
	880FH	Dot Data	Dot Data
X81	8810H	OBJ Code "080" & BG Code "081"	OBJ Code "180" & BG Code "181"
	881FH	Dot Data	Dot Data
Area shared by OBJ and BG			
XFE	8FE0H	OBJ Code "0FE" & BG Code "0FE"	OBJ Code "1FE" & BG Code "1FE"
	8FEFH	Dot Data	Dot Data
XFF	8FF0H	OBJ Code "0FE" & BG Code "0FF"	OBJ Code "1FE" & BG Code "1FF"
	8FFFH	Dot Data	Dot Data
X00	9000H	BG Code "000"	BG Code "100"
	900FH	Dot Data	Dot Data
X7F	97F0H	BG Code "07F"	BG Code "17F"
	87FFH	Dot Data	Dot Data

CHR Codes:

- OBJ 128 x 2 type
- BG 256 x 2 type

2) When the BG character data are assigned to addresses 8000~8FFFH, it is the same area as the OBJ, and the character dots which correspond with the CHR code also become the same.

OBJ (Objects)

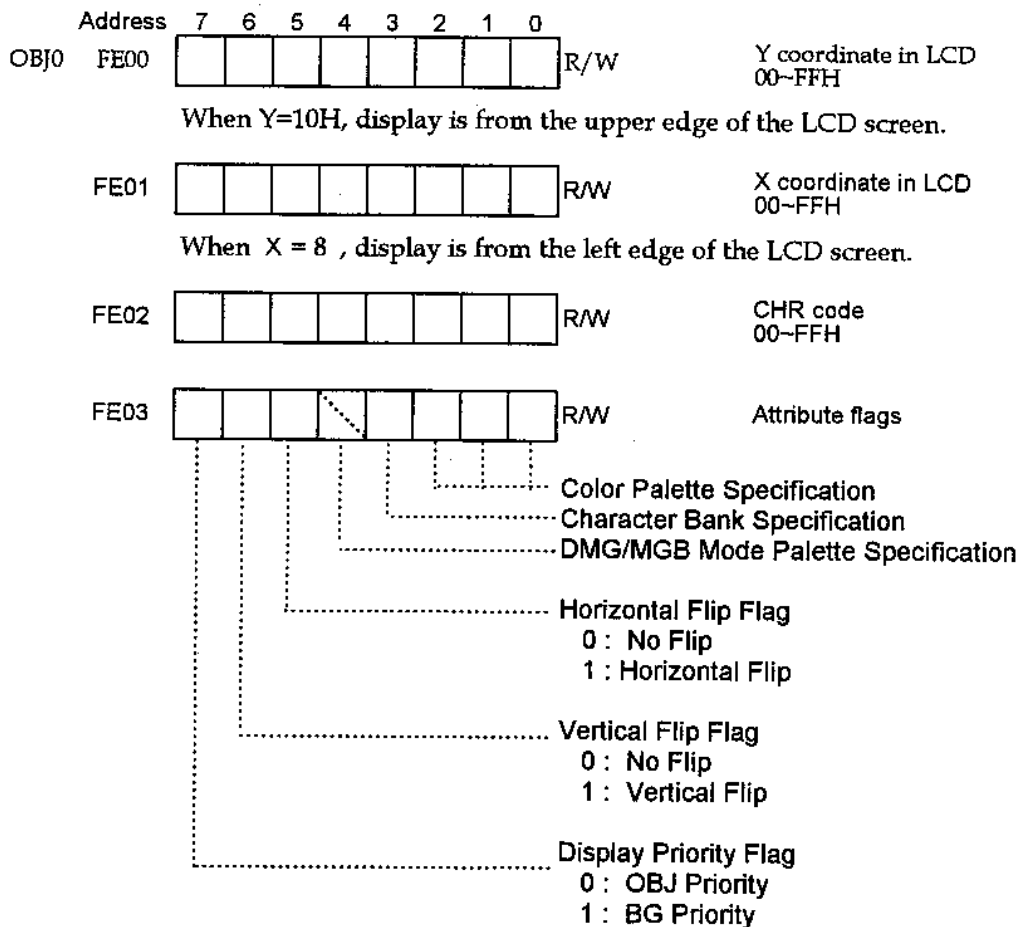
40 OBJ (Objects) worth of data can be written to the OAM-RAM inside the LSI, so that 40 OBJ can be displayed on the LCD screen. Up to 10 OBJ can be displayed on the same Y line.

One OBJ datum consists of a total of 32 bits comprising the Y coordinate (8 bits), X coordinate (8 bits), CHR code (8 bits), BG/OBJ display priority (1 bit), vertical flip (1 bit), horizontal flip (1 bit), DMG/MGB mode palette specification (1 bit), character bank specification (1 bit), and color palette specification (3 bits).

Whether the OBJ has an 8 x 8 dot or an 8 x 16 dot block configuration per datum can be designated by the LCDC register.

When the OBJ is given an 8 x 16 dot configuration, the CHR code designates an even code, just as with DMG/MGB.

OAM Register



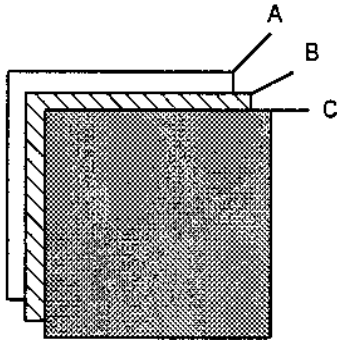
NOTE The DMG/MGB palette is used during DMG/MGB Mode, while the color palette and character bank specification flag are used during CGE Mode.

OBJ1~OBJ39 have the same configuration as OBJ0.

OBJ (Object) Priority Order

When OBJ are overlaid, the OBJ with the newest OBJ number has priority.

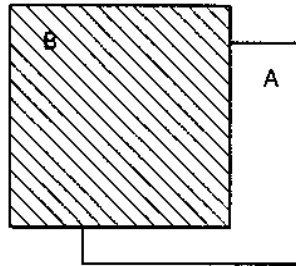
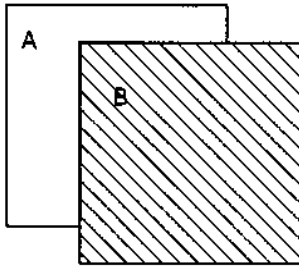
1) When coordinates are all the same



a = No. of OBJ A
 b = No. of OBJ B
 c = No. of OBJ C

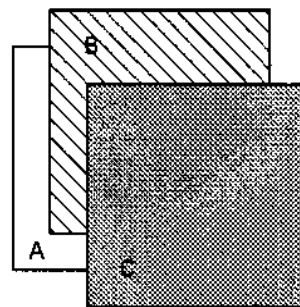
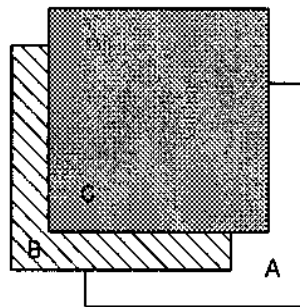
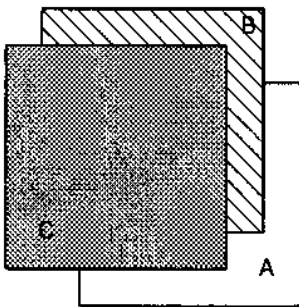
Objects are displayed in this manner when $a > b > c$.

2) When coordinates are different



a = No. of OBJ A
 b = No. of OBJ B
 c = No. of OBJ C

Objects are displayed in this manner when $a > b > c$.



NOTE When in DMG/MGB Mode, the OBJ with the smaller X coordinate has priority only when the X coordinates are different.

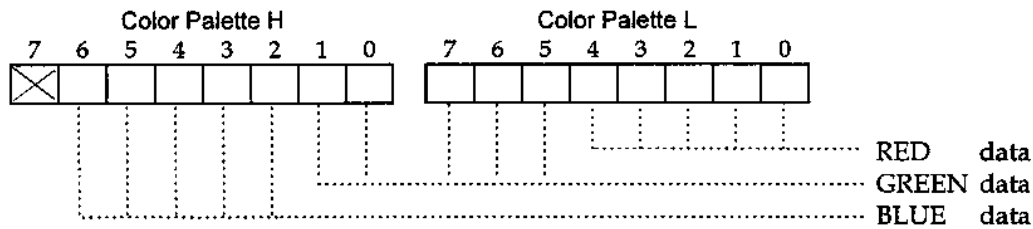
LCD Color Display

A total of 32,768 colors, 32 gradient levels of each R, G, and B, can be displayed by the LCD unit of the CGB system.

A color palette comprises 4 colors selected from among 32,768 colors, and BG and OBJ both can be freely selected from 8 palettes per each character unit. However, since the OBJ side has transparent data, there are 3 colors per one color palette. The color palettes exist independently for BG and OBJ.

Color Palettes

- There are 8 color palettes available for each BG and OBJ. (Palette Nos. 0~7)
- Each palette comprises 4 colors, and is designated by the display dot data (2 bits).
(Palette data Nos. 0~3)
- A color palette has 5 bits of data per RGB color, at a correlation of 2 bytes per 1 dot.
(32,768 colors can be displayed)



Color Palette Configuration

Color Palette No.	Color Palette		Palette Data No.
Color Palette 0	Color Palette H00	Color Palette L00	0
	Color Palette H00	Color Palette L00	1
	Color Palette H00	Color Palette L00	2
	Color Palette H00	Color Palette L00	3
Color Palettes 1~7			

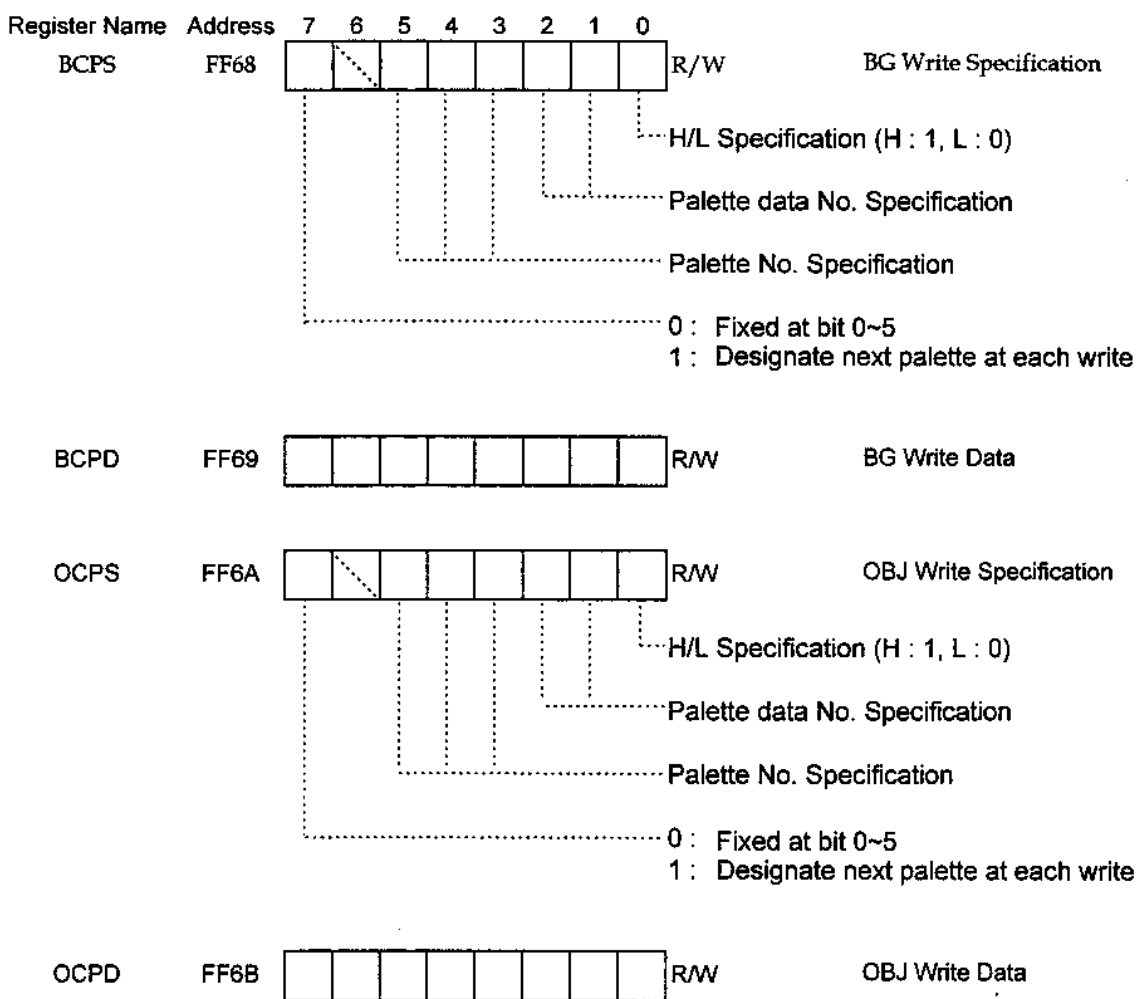
Writing Data to Color Palettes

Writing data to a color palette is accomplished using the write specification register and the write data register.

The write address is specified in the least significant 6 bits of the write specification register. When data are written to the write data register, the data are written to the address specified in the write Specification register. At this time, if a "1" is set in the most significant bit of the write specification register, the write address is automatically incremented, designating the next address. (The next address is read from the least significant 6 bits of the write specification register.)

Reading data from a color palette similarly uses the write specification register and the write data register.

When reading the write data register, data are read at the address specified in the write specification register. During a read, the designated address will not automatically be incremented, even if a "1" is set in the most significant bit of the write specification register.



Overlaying OBJ, BG

Display overlaying an OBJ and a BG during OBJ display is accomplished according to the OBJ display priority flag and the BG display priority flag, as shown in the following table.

Display Priority Flag		Data		Display	
BG	OBJ	OBJ	BG	Palette	Data
"0"	"0"	0	0	BG	0
		0	bg	BG	bg
		obj	0	OBJ	obj
		obj	bg	OBJ	obj
	"1"	0	0	BG	0
		0	bg	BG	bg
		obj	0	OBJ	obj
		obj	bg	BG	bg
"1"	x	0	0	BG	0
	x	0	bg	BG	bg
	x	obj	0	OBJ	obj
	x	obj	bg	BG	bg

x : DON'T CARE

- 0 data in OBJ or BG is expressed as 2-bit data "00."
- obj and bg represent data ("01", "10", "11") for OBJ and BG.
- The OBJ and BG priority is set by the attribute flag in the OBJ OAM (the OBJ display priority flag).

Display when Using an Existing DMG/MGB Game Pak (DMG/MGB Mode)

When an existing DMG/MGB-dedicated (not CGB-compatible) Game Pak is used, coloring is automatically performed by the system utilizing the BGP, OBP0, and OBP1 registers. However, the BG display can use 4 colors, and the OBJ display can use 2 palettes of 3 colors each, excluding transparent data. (A maximum of 10 colors in one screen.)

1) BG Display

Dot data (2 bits) from BGP are displayed in colors specified by BG color palette No. 0.

2) OBJ Display

Dot data (2 bits) from OBP0 and OBP1 are displayed in colors specified by each of the OBJ color palettes No. 0 and No. 1.

The colors which are displayed are automatically selected by the CGB according to palettes which are already registered in the CGB. (They cannot be changed by the program.)

It is also possible for the player to change the palette during the game. However, the palette must be selected from the palettes registered in the CGB.

Changing the palette is accomplished by generating a hardware interrupt by the player simultaneously pressing specific keys during the game, thereby placing the game in a state in which the palette change menu pops up.

This function is enabled only in the DMG/MGB Mode.

CPU Operating Speed

The CGB-CPU is able to switch operating speeds according to the application.

In Normal Mode, each block operates at exactly the same speed as a DMG/MGB-CPU. In Double Speed Mode, all operating speeds double, with the exception of the liquid crystal control circuit and the sound circuit.

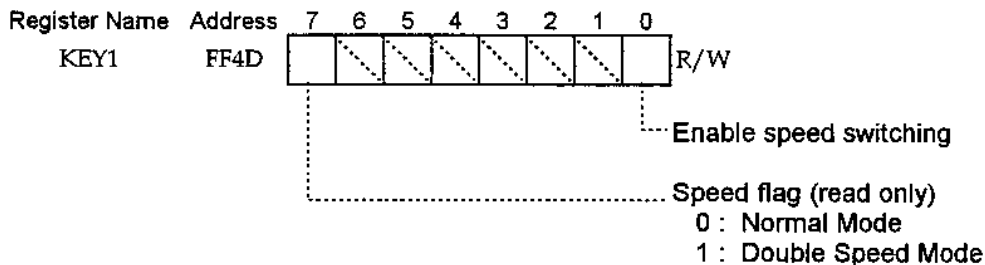
Normal Mode	1.05 MHz (CPU system clock)
Double Speed Mode	2.10 MHz (CPU system clock)

Switching CPU Operating Speeds

Immediately after resetting the CGB-CPU (immediately after Reset Clear), the system operates in Normal Mode.

Switching the CPU operating speed is accomplished by executing the "STOP" command while the 0 bit of the [KEY1] register is set to "1". When this operation is executed in Normal Mode, the status shifts to Double Speed Mode. If this operation is executed in Double Speed Mode, the status shifts to Normal Mode. Bit 0 of the [KEY1] register is automatically reset after switching the CPU operating speed.

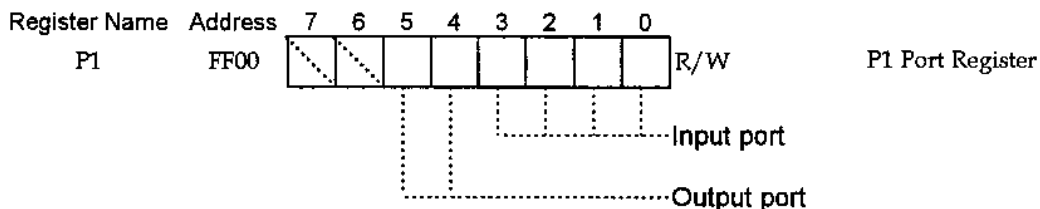
In addition, bit 7 of the [KEY1] register is the CPU speed flag and indicates the current CPU speed.



NOTE When a "1" is set in bit 0 of the [KEY1] register, the standby function cannot be used. When using the standby function, be sure to use the function after confirming that a "0" is set in bit 0 of the [KEY1] register.

When performing this operation, after resetting all of the interrupt enable flags, just as when executing the standby function (STOP Mode), execute the STOP command with a "1" set in bit 4 and bit 5 of the P1 port register.

Since operation will automatically return from the STOP Mode with this operation, there is no need to create a cause to cancel the STOP mode, but until the CPU operating speed is changed and the system clock is restored, keep a "1" in bit 4 and bit 5 of the P1 port register.

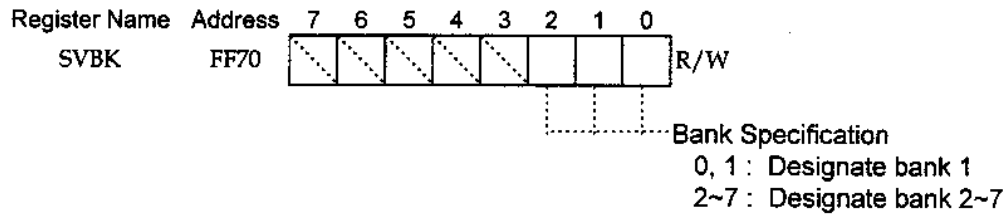


A mask ROM which is compatible with the Double Speed Mode is necessary to use the Double Speed Mode.

In addition, the battery life is shortened when the Double Speed Mode is used.

Work Memory Bank Register

The CGB work memory (32 Kbytes) is divided into 8 banks in 4 Kbyte units. Addresses C000~CFFFH in the CPU memory space are fixed for bank 0, while addresses D000~DFFFH are for switching between banks 1~7. The least significant 3 bits of the [SVBK] bank register are used for switching. (When "0" is specified, bank 1 is selected.)



DMA Transfer

Old DMA Transfer

A DMA transfer will transfer only 40 x 32 bits worth from addresses 0~DFFFH to the OAM (addresses FE00~FE8FH). The transfer start address can be designated for each 100H addresses, for addresses 0~DFFFH.

The transfer method is the same as that for DMG/MGB. But when transferring from addresses 8000~9FFFH (display RAM area), the data inside the bank designated by bit 0 of the [VBK] register are transferred. In addition, when transferring from addresses D000~DFFFH (CGB work RAM area), the data inside the bank designated by the 3 least significant bits of the [SVBK] register are transferred.

When the CPU operating speed is doubled, the transfer speed is also doubled.

New DMA Transfer

In addition to the DMA transfer which is built into existing DMG/MGB, the following DMA transfer functions have been added.

1) Horizontal Blanking DMA Transfer

This automatically transfers 16 bytes of data from the user program area (addresses 0~7FFFH) and the external & CGB work RAM area (addresses A000~DFFFH) to the LCD display RAM area (addresses 8000~9FFFH) at each horizontal blanking period. The number of lines DMA transferred at a horizontal blanking period can be specified from 1 to 128 by setting the [HDMA5] register. CPU processing is suspended during the DMA transfer period.

2) General Purpose DMA Transfer

This transfers from 16 bytes to 2048 bytes (can be set in 16-byte increments) of data from the user program area (addresses 0~7FFFH) and the external & CGB work RAM area (addresses A000~DFFFH) to the LCD display RAM area (addresses 8000~9FFFH). As with horizontal blanking DMA transfer, CPU processing is suspended during the DMA transfer period.

The transfer source CGB work RAM area (addresses D000~DFFFH) is from the bank designated by the SVBK register.

The transfer destination LCD display RAM area (addresses 8000~9FFFH) is from the bank designated by the VBK register.

NOTES The number of bytes transferred in the new DMA transfer is in 16-byte units. Only units which are multiples of 16 bytes can be transferred.

The new DMA transfer operates at a constant speed, regardless of whether the CPU is in Normal or Double Speed Mode.

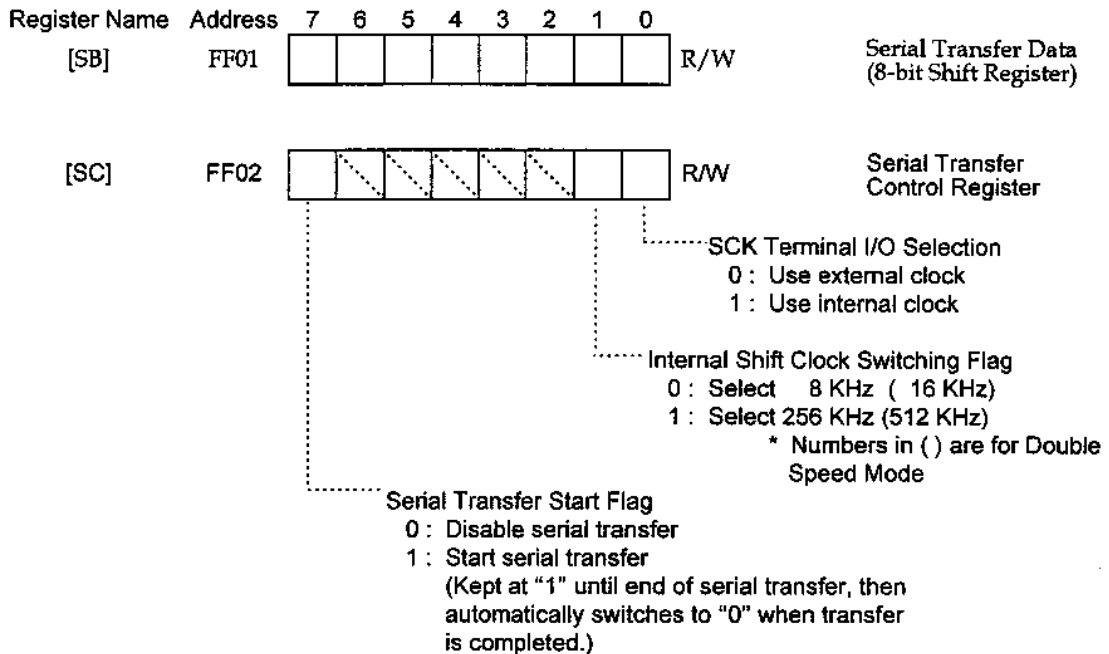
A mask ROM which is compatible with the Double Speed Mode is necessary to use the Double Speed Mode.

New DMA Control Registers

Register Name	Address	7	6	5	4	3	2	1	0		
HDMA1	FF51									W	Transfer Source Specification 00~7FH (Program ROM) A0~DFH (External & Game Work RAM)
HDMA2	FF52									W	Transfer Source Specification 0X~FXH Combined with HDMA1, designates the 12 most significant bits of the transfer source area (000X~7FFXH or A00X~DFFXH)
HDMA3	FF53									W	Transfer Destination Specification 00~1FH
HDMA4	FF54									W	Transfer Destination Specification 0X~FXH Combined with HDMA3, designates the 9 most significant bits of the transfer destination area (800X~9FFXH)
HDMA5	FF55									R/W	Transfer Start and Transfer Quantity (n) During horizontal blanking DMA Number of lines in DMA transfer (n+1) Total number of bytes transferred = 16 x (n+1) (MAX : 2,048 bytes) During general purpose DMA transfer Total number of bytes transferred = 16 x (n+1) (MAX : 2,048 bytes) When "1" is written After "1" is written, horizontal blanking DMA transfer is started according to initial horizontal blanking period. * If "0" is then written, DMA transfer stops according to the next horizontal blanking period. When "0" is written When "0" is written (When this bit is "0", this is limited to when "0" has already been written) Start general purpose DMA transfer * General purpose DMA transfer cannot be stopped or suspended except by inputting a reset signal.

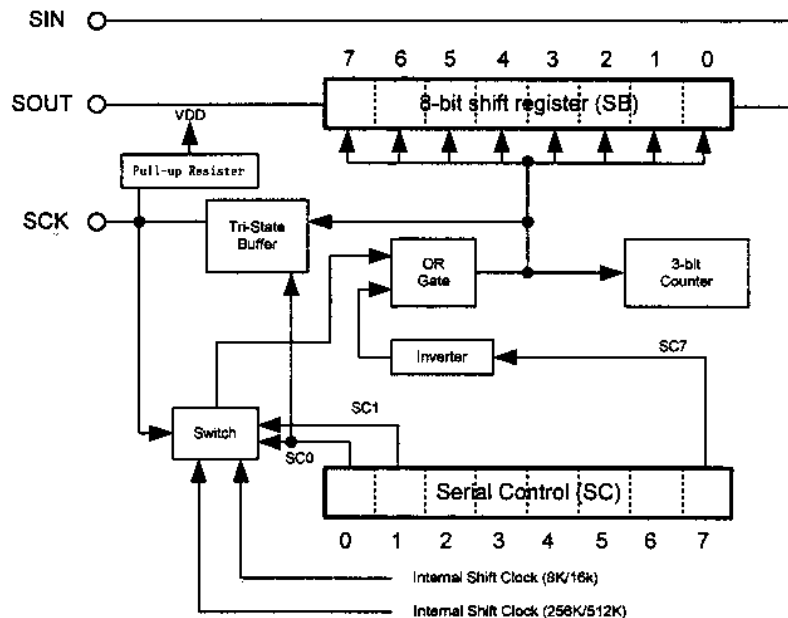
Serial Input/Output (SIO)

Serial input/output are basically the same as for the DMG/MGB, except that the internal shift clock operating speed can be switched by specification bit 1.



When using a DMG/MGB dedicated Game Pak, the internal clock will be used at 8KHz, regardless of the content of bit 1 of the SC register.

SIO Block Schematic



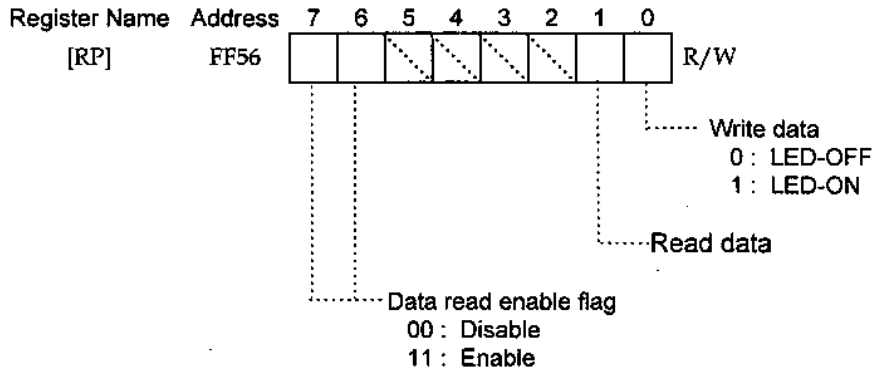
Infrared Communications Port

The SGB System is equipped with an infrared communications function.

An infrared signal can be output by writing data to bit 0 of the RP register.

In addition, any received infrared signal is latched inside the LSI to the rise of the system clock. Latched data can then be read from bit 1 of the RP register by setting bit 6 and bit 7 of this register to "1".

To conserve power, set the value of the RP register to 00H when not sending or receiving data.



* Initial value of RP register : 00H

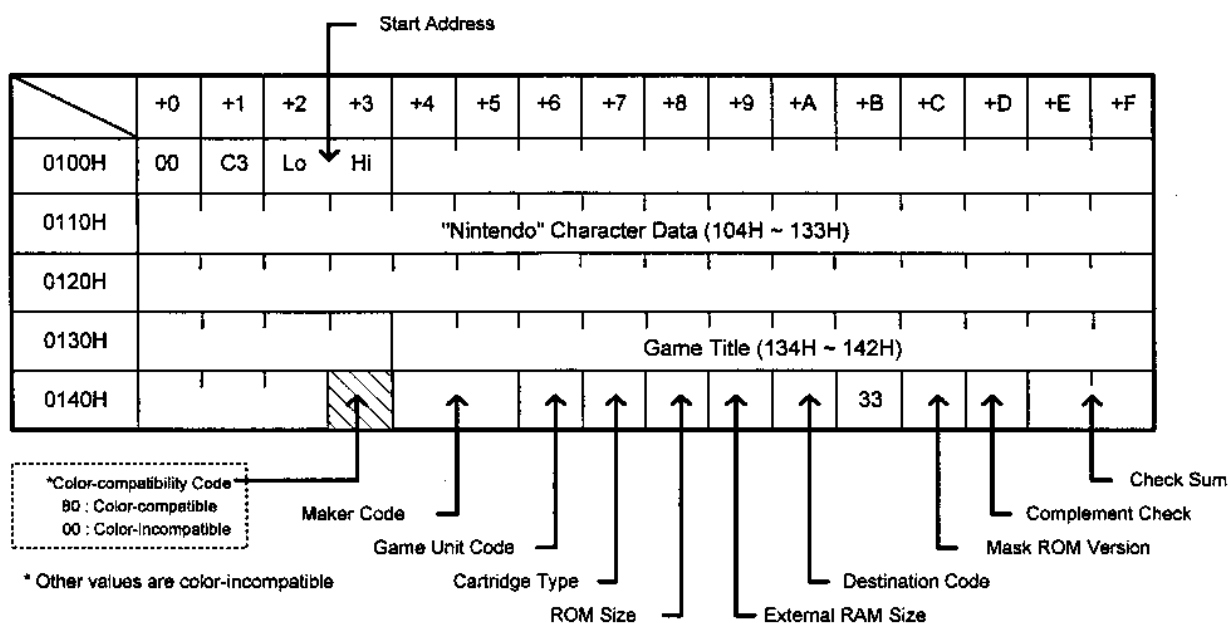
Appendix A

Specifications of Data Registered in ROM

In CGB programs, as with conventional DMG/MGB-dedicated programs, it is necessary to set data pertaining to the game name and Game Pak specifications in the 80 bytes comprising addresses 100~14FH in the CPU memory.

However, please set a new code pertaining to color-compatibility at address 143H to identify whether the program is a color-compatible program.

If "80" is set at address 143H, the system recognizes the program as a color-compatible program. Otherwise, if "00" or any value other than "80" (existing DMG Game Pak) is stored at this address, it will be recognized as color-incompatible (conventional DMG program).



Color-compatible : When using CGB, a maximum of 56 colors can be displayed in one screen

Color-incompatible : When using CGB, a maximum of 10 colors can be displayed in one screen

Store fixed values in the following addresses, regardless of the game.

- Address 100H = 00H
- Address 101H = C3H
- Address 14BH = 33H
- Addresses 104H~133H = "Nintendo" character data

Example of Creating Software for CGB

When creating software for the CGB, set the color-compatibility code in the ROM registration data area and use the branching method inside the program according to the hardware.

(See Flow Chart 1)

However, if the functions which are used are limited as in the following example, processing can be normalized without branching.

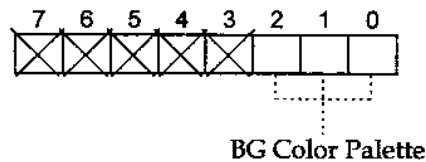
(See Flow Chart 2)

As Program Example 1, the method for creating software which will operate on all CGB and DMG/MGB model games, and which can display 56 colors when used on CGB will be explained. If a similar method is used, it is possible to maintain compatibility with old hardware (DMG/MGB), while using the CGB functions.

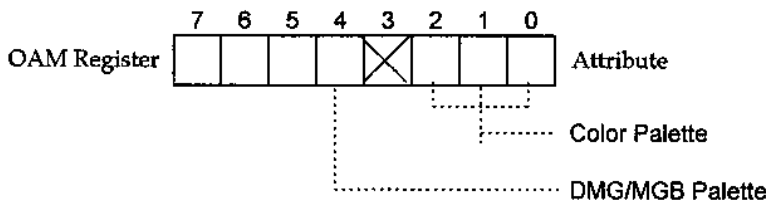
Program Specifications

- Use only character dot data bank 0.
- Use only the BG attribute color palette (bits 0~2 in bank 1).

	Bank 0	Bank 1
8000H	Character Dot Data	X Character Dot Data X
9800H	BG CHR Code	BG Attribute
9C00H 9FFFH	BG CHR Code	BG Attribute



- Set both the color palette and the DMG/MGB palette in the attribute flags of the OAM register.



- Otherwise, do not use any of the expanded functions specific to the CGB.

Recognizing CGB

The following methods are used to determine on which model (DMG (SGB), MGB (SGB2), or CGB) a program is running.

- This is determined by the value in the accumulator (A register) in the CPU.

- 01H → DMG (SGB)

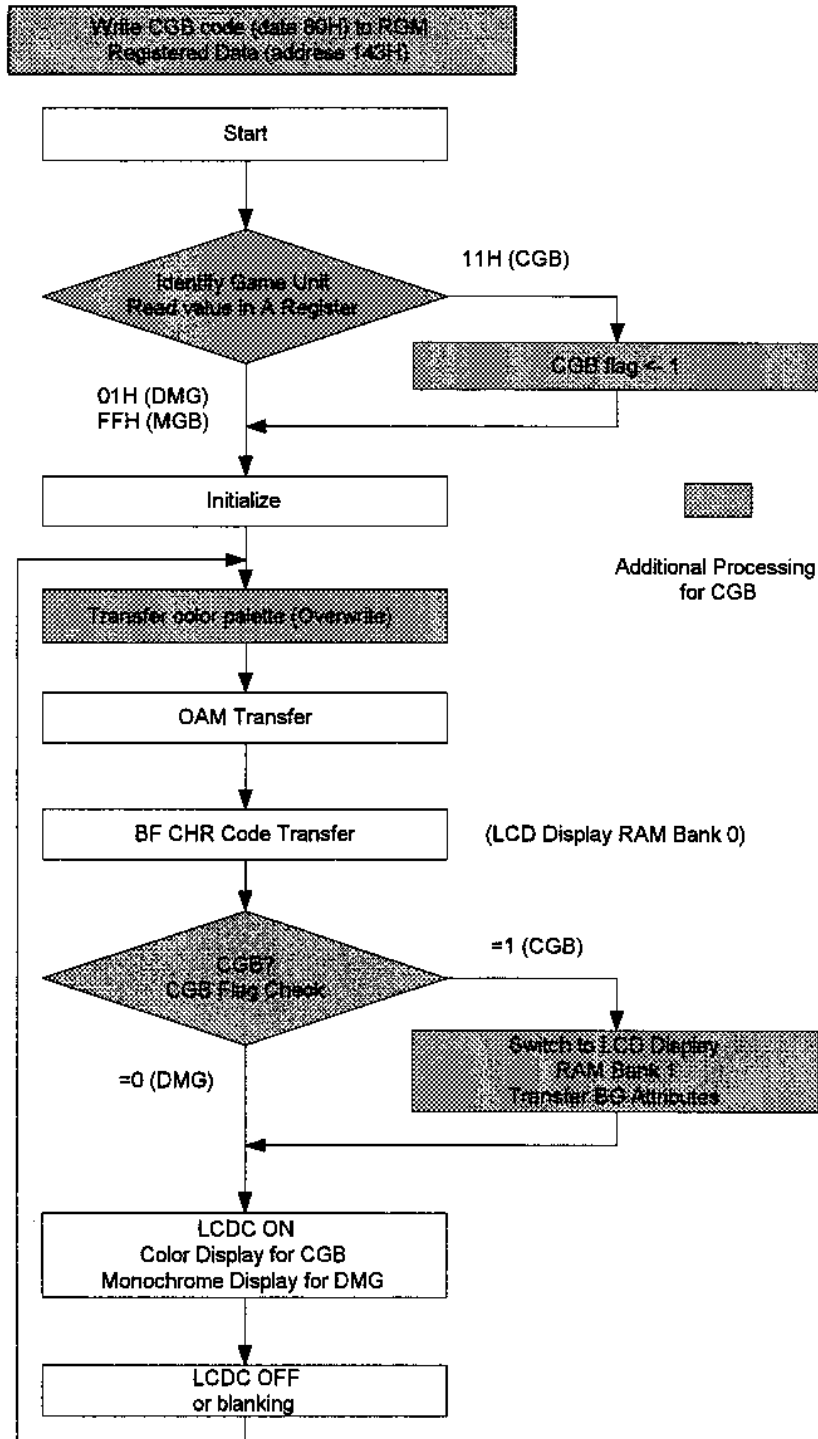
- FFH → MGB (SGB2)

- 11H → CGB

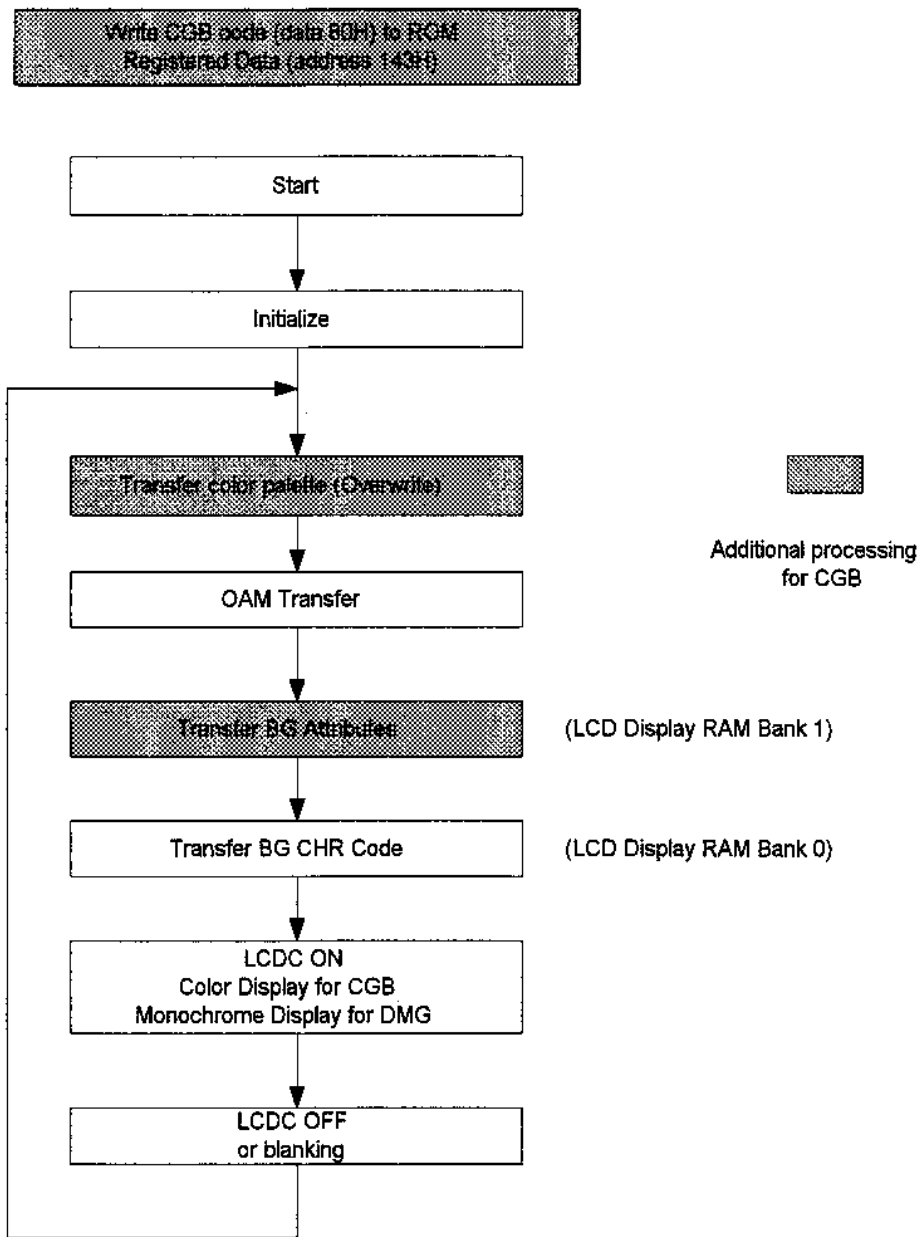
- * See the Super NES Development Manual for information concerning SGB determination.

Flow Charts

Branch Processing for the CGB and DMG/MGB



Normal Processing for the CGB and DMG/MGB



NOTES Be sure to transfer BG attributes first.

After attributes transfer, be sure to transfer the CHR code from the same address, even if only the BG attributes are changed.

CGB Control Registers

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Comments
P1 Port P15-P10	FF00			P15	P14	P13	P12	P11	P10	R/W Transfer data control at P14 P15
SB Serial Transfer Register	FF01									R/W Transfer data
SC Serial Control	FF02	Transfer Start 0: No 1: Start						Clock Speed 0: 8 KHz 1: 256 KHz	Shift Clock 0: External 1: Internal	R/W
DIV Divider	FF04	$f/2^{18}$ 64 Hz	$f/2^{18}$ 128 Hz	$f/2^{14}$ 256 Hz	$f/2^{13}$ 512 Hz	$f/2^{12}$ 1024 Hz	$f/2^{11}$ 2048 Hz	$f/2^{10}$ 4096 Hz	$f/2^8$ 8192 Hz	R/W Cleared by LC command to this register
TIMA Timer	FF05									R/W Timer game unit
TMA Timer Module	FF06									R/W Timer preset register
TAC Timer Control	FF07						Timer Stop 0: Stop 1: Run	Frequency Selection Bit 00: $f/2^2$ 10: $f/2^4$ 01: $f/2^4$ 11: $f/2^8$		R/W
IF Interrupt Request Flag	FF0F				P10 - P13 Terminal Fail	Serial Transfer End	Timer Overflow	LCDC Controller STAT	Vertical Blanking	R/W Bit reset enable
IE Interrupt Enable Flag	FFFF				P10 - P13 Terminal Fail	Serial Transfer End	Timer Overflow	LCDC Controller STAT	Vertical Blanking	R/W 0: Disable 1: Enable
IME Interrupt Master Enable										Set with DI, reset with EI 0: Prohibit interrupt 1: Enable interrupt
LCDC LCDC Control	FF40	Controller 0: Stop 1: Run	WIN Bank 0: 8000- 1: 9C00-	Window 0: OFF 1: ON	BG Character 0: 8000- 1: 8000-	BG Bank 0: 9500- 1: 9C00-	OBJ Structure 0: 8 x 8 1: 8 x 16	OBJ Display 0: OFF 1: ON	BG Display 0: OFF 1: ON	R/W Make same area as OBJ by setting 1 in bit 4
STAT LCDC Status Information	FF41		Select LCDC Match Flag	Select Status Interrupt Mode 10	Select Selection Flag Mode 01	Select Mode 00	LYC Match 0: 1: LYC-LY	Mode 00: RAM Access 10: OBJ Search 01: V Blanking 11: LCD Transfer		R/W Bits 3-6 Interrupt 0: Not selected 1: Selected
SCY Scroll Y Register	FF42									R/W 00H - FFH
SCX Scroll X Register	FF43									R 00H - FFH
LY LCDC Y Coordinate	FF44									R Y coordinate in display
LYC LY Compare Register	FF45									R/W Match flag is set when LYC=LY
DMA DMA Transfer	FF46									W 00H - DFH Transfer starts at the same time that address is set

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Comments	
BGP PG Palette Data	FF47	Character Dot Data 11 Palette Data when in DMG/MGB Mode	Character Dot Data 10 Palette Data when in DMG/MGB Mode	Character Dot Data 09 Palette Data when in DMG/MGB Mode	Character Dot Data 08 Palette Data when in DMG/MGB Mode	Character Dot Data 07 Palette Data when in DMG/MGB Mode	Character Dot Data 06 Palette Data when in DMG/MGB Mode	Character Dot Data 05 Palette Data when in DMG/MGB Mode	Character Dot Data 04 Palette Data when in DMG/MGB Mode	W	
OBP0 OBJ Palette Data 0	FF48	Character Dot Data 11 Palette Data when in DMG/MGB Mode	Character Dot Data 10 Palette Data when in DMG/MGB Mode	Character Dot Data 09 Palette Data when in DMG/MGB Mode	Character Dot Data 08 Palette Data when in DMG/MGB Mode	Character Dot Data 07 Palette Data when in DMG/MGB Mode	Character Dot Data 06 Palette Data when in DMG/MGB Mode	Character Dot Data 05 Palette Data when in DMG/MGB Mode	Character Dot Data 04 Palette Data when in DMG/MGB Mode	W When attribute bit 4 is 0	
OBP1 OBJ Palette Data 1	FF49	Character Dot Data 11 Palette Data when in DMG/MGB Mode	Character Dot Data 10 Palette Data when in DMG/MGB Mode	Character Dot Data 09 Palette Data when in DMG/MGB Mode	Character Dot Data 08 Palette Data when in DMG/MGB Mode	Character Dot Data 07 Palette Data when in DMG/MGB Mode	Character Dot Data 06 Palette Data when in DMG/MGB Mode	Character Dot Data 05 Palette Data when in DMG/MGB Mode	Character Dot Data 04 Palette Data when in DMG/MGB Mode	W When attribute bit 4 is 1	
WY Window Y Coordinate	FF4A									R/W 0 - 143 Upper edge when WY=0	
WX Window X Coordinate	FF4B									R/W 7 - 166 Left edge when WX=7	
KEY 1 CPU Speed Switching	FF4D	Speed 0 : Normal 1 : Double							Enable Speed Switching	R/W When bit 0 is set to 1, switch when STOP command is executed	
VBK VRAM Bank Specification	FF4F								Bank Specification 0 : Bank 0 1 : Bank 1	R/W Bank 0 is selected immediately after reset signal is canceled	
HDMA1 Horizontal Blanking, General Purpose DMA Control	FF51									W 00H - 7FH (ROM) A0H - DFH (WRAM)	
HDMA2 Horizontal Blanking, General Purpose DMA Control	FF52									W 0XH - FXH	
HDMA3 Horizontal Blanking, General Purpose DMA Control	FF53									W 00H - 1FH	
HDMA4 Horizontal Blanking, General Purpose DMA Control	FF54									W 0XH - FXH	
HDMA5 Horizontal Blanking, General Purpose DMA Control	FF55	DMA Selection 0 : General Purpose 1 : H Blanking	Number of lines in DMA transfer during H Blanking DMA								W General Purpose DMA stops on reset. H Blanking DMA stops when bit 7 is set to 0
RP Infrared Communications Port	FF56	Data Read Enable Flag 00 : Disable 11 : Enable						Read Data	Write Data	R/W	
BCPS Color Palette BG Write Specification	FF68	Increment 0 : OFF 1 : ON		Palette No. 0 - 7			Palette Data No. 0 - 3		H/L Specification 0 : L 1 : H		R/W Automatic increment disabled during read
BCPD Color Palette BG Write Data	FF69									R/W	
OCPS Color Palette OBJ Write Specification	FF6A	Increment 0 : OFF 1 : ON		Palette No. 0 - 7			Palette Data No. 0 - 3		H/L Specification 0 : L 1 : H		R/W Automatic increment disabled during read
OCPD Color Palette OBJ Write Data	FF6B									R/W	
SVBK VRAM Bank Specification	FF70						Bank Specification 0, 1 : Designate Bank 1 2-7 : Designate Bank 2-7			R/W	

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Comments
OBJ0 ^{*1} (Same for 1-39) LCD Y Coordinate	FE00									R/W 00H - FFH Y=10H is upper edge
LCD X Coordinate	FE01									R/W 00H - FFH X=08H is upper edge
Character Code	FE02									R/W 00H - FFH
Attribute Flags	FE03	Display Priority 0: OBJ 1: BG	Vertical Flip 0: Normal 1: Flip	Horiz. Flip 0: Normal 1: Flip	Palette specification during DMG/MGB Mode	VRAM Bank 0: Bank 0 1: Bank 1	Color Palette No. 0 - 7			R/W
^{*1} OBJ1 - OBJ39 are the same as OBJ0										

Sound Registers

The sound registers are entirely the same as those for the DMG/MGB System.
(See the Game Boy Development Manual)

Memory Controllers

- The following Memory Controller ICs have been manufactured for the purpose of memory management. MBC-1, MBC-2, and MBC-3 are compatible with both Game Boy and Game Boy Color.

MBC-1 INSTRUCTIONS

EXPANSION

- MBC-1 is a memory controller which uses 512 Kb (64 Kb) or more of ROM and 256 Kb (32 Kb) or more of RAM, under the following conditions.

WHEN CONTROLLING UP TO 4M BITS OF ROM

When controlling up to 4M bits (512 Kb) of ROM, up to 256 Kb (32 Kb) of RAM can be controlled.

WHEN CONTROLLING 8M OR MORE OF ROM

8Mbits or more of ROM can be controlled under the following conditions.

When controlling 8M bits of ROM, the ROM addresses 080000 ~ 083FFFh (bank 20h) cannot be used.

When controlling 16M bits of ROM, the ROM addresses 080000 ~ 083FFFh (bank 20h), 100000 ~ 103FFFh (bank 40h), and 180000 ~ 183FFFh (bank 60h) cannot be used.

Only 64 Kb (8 Kb) of RAM can be used.

MBC-3 INSTRUCTIONS

- The MBC-3 is a memory controller which uses up to 16M bits (2M bytes) of ROM, and 256 Kb (32 Kb) of RAM. It includes an external Quartz Oscillator (32.768 KHz). The clock counter is built into the MBC-3.

CONTROL REGISTERS

REGISTER-0

Function: RAM and clock counter write protect (default: 0)

Address: 0000 ~ 1FFFh

Data to be written: 0Ah

Note: Access to RAM and clock counter registers is enabled.

REGISTER-1

Function: ROM bank code (default: select 0~ROM bank 1)

Address: 2000 ~ 3FFFh

Data to be written: 1~7Fh

Note: ROM banks can be selected in 16 KB units.

REGISTER-2

Function: RAM bank code (default: select 0~RAM bank 0)

Address: 4000 ~ 5FFFh

Data to be written: 0~3

Note: RAM banks can be selected in 8 KB units.

Function:

Address: 4000 ~ 5FFFh

Data to be written: 8 ~ Ch

Note: The clock counter can be selected.

Clock Counter Register

Data	Register	Value Range	Function
8	RTC S	0-69 (0-3Bh)	Second counter (8 bits)
9	RTC M	0-59 (0-3Eh)	Minutes counter (6 bits)
Ah	RTC H	0-23 (0-17h)	Hour counter (5 bits)
Bh	RTC DL	0-255 (0-FFh)	Lower 8 bits of day counter
Ch	RTC DH	Bit 7: <input type="checkbox"/> Bit 6: <input type="checkbox"/> Bit 5: <input type="checkbox"/> Bit 4: <input type="checkbox"/> Bit 3: <input type="checkbox"/> Bit 2: <input type="checkbox"/> Bit 1: <input type="checkbox"/> Bit 0: <input type="checkbox"/>	Upper 1 bit of day counter and day counter carry bit
			Bit 0: Most significant bit of day counter Bit 6: HALT Bit 7: Day counter carry bit
HALT - controls start/stop of clock counter			

■ The day counter consists of a 9-bit counter and a carry bit, enabling counting from 0 to 511 (0 ~ 1FFh) possible. When the carry bit is "1" it remains "1" until a "0" is written. The counter starts when HALT is "0" and stops when HALT is "1." Numeric values outside the range of each counter result in incorrect writing.

REGISTER-3

Function: Latches all clock counter data

Address: 6000 ~ 7FFF

Data to be written: 0 → 1

Note: When 0 → 1 is written, all clock counter data is latched. Data remains latched until 0 → 1 is written again.

ACCESSING THE CLOCK COUNTER

- Each register of the clock counter is assigned an address in the CPU's external extended RAM. To access the clock counter, the RAM Bank must first be switched on. (Register - 0)
- External Extended RAM Area (A000-BFFFh) Bank Map

External Extended RAM Area (A000-BFFFh) Bank Map

Bank	Device	Remarks
0	RAM bank 0	
1	RAM bank 1	
2	RAM bank 2	
3	RAM bank 3	
8	RTC S	Not Used
9	RTC M	
Ah	RTC H	
Bh	RTC DL	
Ch	RTC DH	
-	-	Not Used

- The following examples describe various ways to access the clock counter.

READING

Write "0Ah" to register 0, to open the gate for access. To read the clock counter value, set register 3 to "1" (this will latch the values of all registers). If register 3 is already set to "1," reset it to "0" then back to "1."

While register 3 is set to "1," the values of all latched clock counter registers will not change, allowing you to read its values, while the clock counter continues to run.

For example, to access the "RTC S register," set the RAM bank to "8." The value of the RTC S register can then be accessed by reading any CPU address from A000h to BFFFh.

WRITING

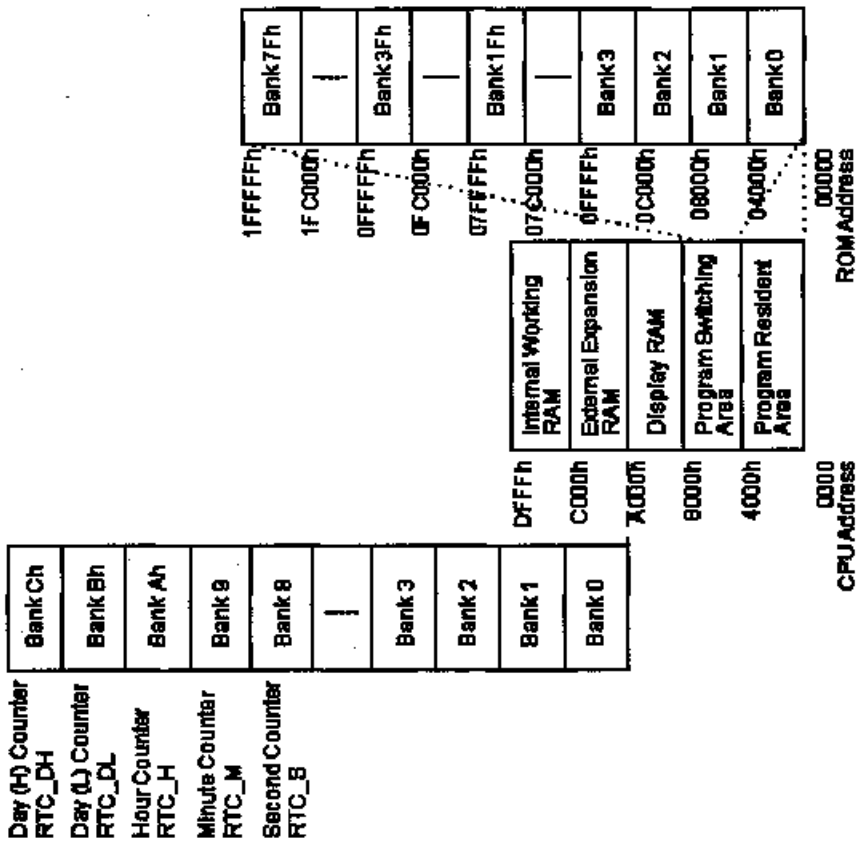
Writing "0Ah" to register 0 will open the gate for access, allowing you to write to each register of the clock counter.

PRECAUTIONS WHEN ACCESSING THE CLOCK COUNTER

The clock counter is asynchronously accessed from the CPU. The MB-C3 is equipped with an interface circuit for the WR signal from the CPU. This interface will result in delays when accessing the various RTC S, RTC M, RTC H, RTC DL, and RTC DH registers. If accessing these registers on a continuous basis, it is important to enter a 4-cycle delay between them.

MEMORY MAP

- ROM bank "0" is assigned to the program resident area (0 ~ 3FFFh) of the CPU and cannot be changed.
- ROM banks "1" ~ "7Fh" is assigned to the program switching area (4000 ~ 7FFFh) of the CPU memory.
- RAM banks "0" ~ "3," and one of the clock counter registers (RAM banks "8" ~ "Ch") are assigned to the external expansion WRAM (A000 ~ BFFFh) of the CPU memory.



WHEN CONTROLLING 8M BITS OR MORE OF ROM

